neutron diagnostics signals simulation approaches on iter project using gpu [[1]](#footnote-1)\*)

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During the development of digital signal processing modules for neutron diagnostics, it is mandatory to check the correct operation of the processing algorithms. For these purposes, one can use a simulator of signals which is specific to a particular diagnostic system. These simulators are software and hardware systems capable of generating and reproducing signals similar to those of neutron detectors.

Today it is possible to generate waveform files with count rate up to 108 pulses/s. As well the maximum possible count rate is limited up to 106 pulses/s in the "real time" generation mode. This can be explained with the fact that at high count rate the playback time of a signal segment is less than the time of generation and recording of the next segment in the DAC memory.

To be able to generate signals in "real time", it is necessary to reduce the time of data generation. To do this, it is proposed to generate a signal using devices that are more efficient than the CPU ([1] and [2]).

The main feature of systems built on FPGA is the complex calculation of the pulse distribution over time. Since FPGA is a synchronous digital system, generation of Poisson distribution implies usage of additional calculations, and this results in a distribution that is close to Poisson [2]. To get around this objection, it was proposed to use a GPU to generate data.

This report discusses the concept of a neutron diagnostics signal simulator, a computer appliance for generating a signal to a file or in real time. To reduce the data generation time, it is proposed to use an Nvidia graphics processor with CUDA (Compute Unified Device Architecture) technology. Using CUDA allows to use the multi-core architecture of the GPU, which significantly speeds up the calculations, compared to calculations on the CPU. Using CUDA allows you to quickly transfer data from the GPU to the AWG (Arbitrary Waveform Generator) memory for subsequent playback.

This simulator configuration can be implemented in various ways:

• The GPU is located in the PC case. In this case, the DAC can also be located in a PC case or be part of a remote I/O chassis.

• Using a GPU on a CompactPCI board. In this version, the DAC is located on the same CompactPCI bus.

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1. \*) [abstracts of this report in Russian](http://www.fpl.gpi.ru/Zvenigorod/L/E/ru/KB-Nikolaev.docx) [↑](#footnote-ref-1)